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Ultra-low power biosensors: VLSI trends and future scope

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Implantable Medical Devices (IMDs), especially biosensors research is still in its early stages and thus represents an enormous opportunity for which Ultra-Low-Power System on Chip (SoC) and VLSI/MEMS technologies can enable the development of novel devices and therapies. Broadly, biomedical implants encompass a range of medical solutions for various bodily disorders and include cardiovascular implantable devices such as defibrillators, pacemakers; Neural devices like Deep Brain Stimulation (DBS) and prostheses for Central Nervous System (CNS), Peripheral Nervous System (PNS), cochlear and retinal applications; Biosensors include miniaturized glucose sensor, cholesterol sensors, saliva sensors etc. are picking up in the research arena. Unlike other commercial devices however, developing microsystems for these applications requires critical analysis in terms of specifications, technologies and design techniques because of the device's safety and efficacy. The trade-off between performance and power consumption is a challenging act in the design of these devices. This presentation aims to evaluate possible applications, to derive the requirements that future circuits integrating bio-sensors, ultra-low power processors, must meet and to recognize, as far as possible, the challenges which have to be faced.

Recent Publications

1. Suhaib Ahmed and Vipan Kakkar (2017) Modeling and simulation of an 8-bit auto-configurable SAR ADC for cardiac and neural implants. Simulation: Transactions of the Society for Modelling and Simulation International: 1-19.

2. Vikram Kumar and Vipan Kakkar (2017) Miniaturized Resonant Power Conversion for Implanted Medical Devices. DOI 10.1109/ACCESS.2017.2728364, IEEE Access.

Biography

Vipan Kakkar has received his Bachelor's degree in Electronics Engineering from Nagpur University, India, Master's degree from Bradford University, UK and Doctorate from Delft University of Technology, Netherlands. He has worked at Phillips, Netherlands as R&D Engineer and System Architect in various system-onchip projects for 8 years. Presently, he is working as a Faculty in the Department of Electronics Engineering, Shri Mata Vaishno Devi University, India. His research interests include nanotechnology, ultra-low power analog and mixed signal design, Microelectromechanical Systems (MEMS) design, synthesis and optimization of digital circuits, biomedical system and implants design and audio and video processing. He is a Senior Member of the IEEE and Life Member of the ISTE and has served as an Executive Council Member of IEEE, Delhi, India and has developed IPs and published many research papers in peer-reviewed journals and international conferences.

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