Next Generation High Speed Computing Using System-on-Chip (SoC) Technology

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Abstract

System on chip is the most modern form of technology being under use and further research for the high speed applications. This technology has nominated a large number of different research areas which would lead the existing technology towards the one of the most widely used computing technology. This technology has raised many emerging issues and has announced big challenges for the researchers and engineers. They are result of microprocessors, memories, buses systems, communications systems, standards, protocol processors, interfaces and other intellectual property components. Alternatively, a SoC product is designed with the concept of embedded system that is capable of being implemented on a single chip, thereby producing a system which can be placed in any environment which is smaller, faster and more efficient system. In this research paper a most comprehensive survey report of existing SoC technology and its underlying issues has been presented. The paper raises a large number of technical aspects at hardware level as well as software level which should be investigated for further exploration of the technology to demonstrate a high speed performance gain.

Keywords: *High Speed Computing, Homogenous SoC, Heterogeneous SoC, Network on Chip, System on Chip*

1. Introduction To SoC Technology

Significant resources have been used with the vast Performa, the design tasks interlinked with scheming between the edifice blocks of circuits and the gathering of a sufficient supporting circuit logic to comprehend a System-on-Chips (SoCs), System-on-Chip is the integrated system which integrates all of the system circuits on the single chip (SoC) is the most advanced form which uses powerful processors and various peripherals for running Windows and Linux. SoC consists of the embedded hardware and software which controls processors, controllers and other peripherals .SoC chips are first been tested before implementing and if any fault is visualized it is reported to the designer.

SoC creates embedded soft wares for Operating System Simulation Systems and other complex system. This kind of the electrically programmable semiconducting digital device is mostly known as System-on-Chip. Consider the Fig. 1 and Fig. 2 which are showing the homogenous and heterogeneous SoC design concepts.

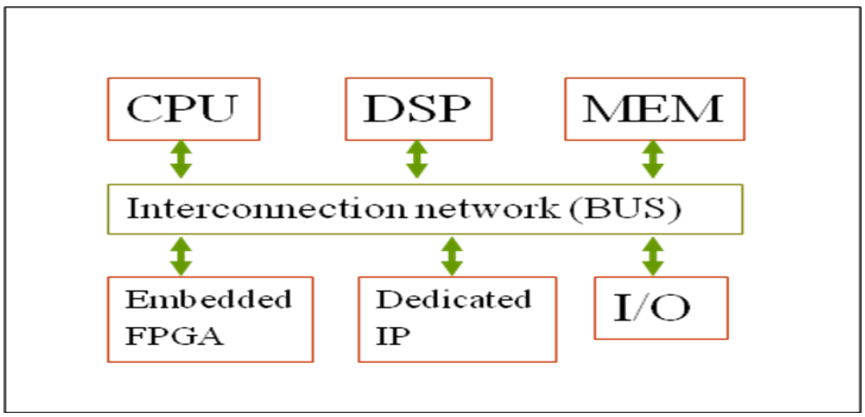

Fig. 1 Heterogeneous SoC

Conventionally System-on-Chips (SoCs) are made by using pre-designed logical models of multi-faceted circuits known as "Circuit Cores" that provide a diversity of applications in computing. These pre-designed serviceable blocks are normally known as "Circuit Cores".

An SOC is composed of its built-in micro-processor circuit core and can also further be composed of one or multiple circuit cores for performing a large number of computing functions. System on-a-chip (SOC) data processors are characteristically based on high degrees of low level integration and are based on a single IC-chip.

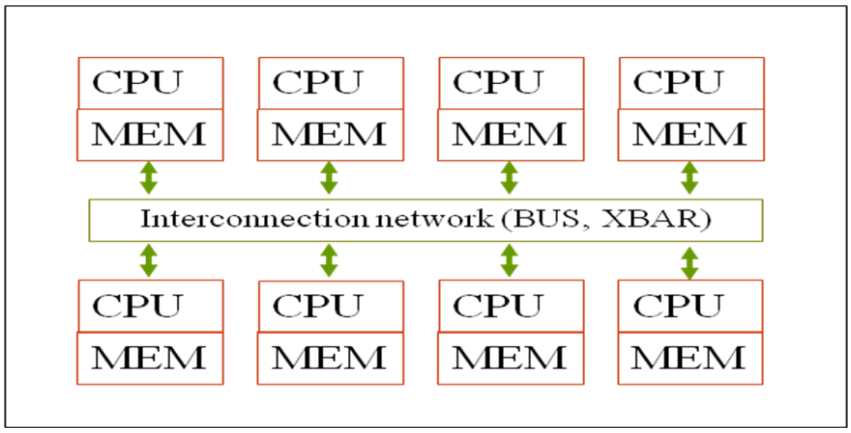

Fig. 2 Homogeneous SoC

2. Top-Down Soc Design Methodology

These flows help to manage the different and conflicting requirements of increasing design size; deep-sub micron affects (DSM) and the necessity for shorter and predictable implementation times. Hierarchical methodologies allow permission to multiple teams to work on different parts of the design concurrently and independently. This "divide and conquer" approach helps reducing the complexity of the design problem for each design team. Consider the Fig. 3 which is showing the top down design approach for SoC systems.

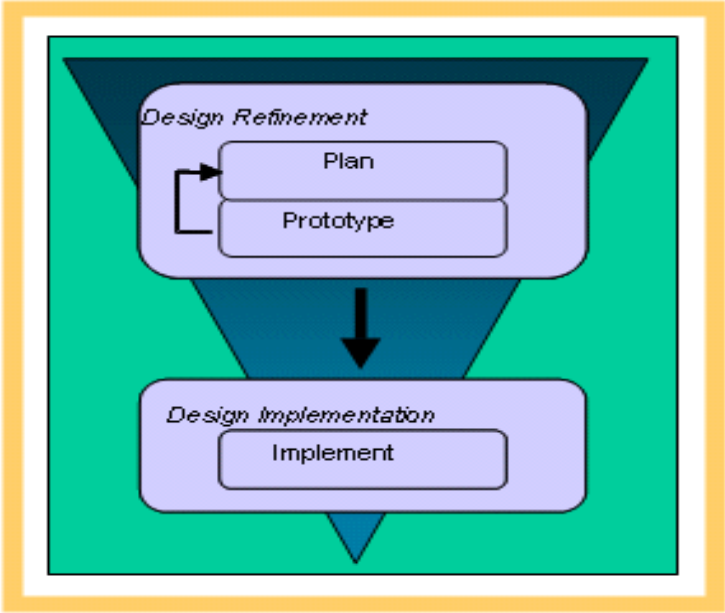

Fig. 3 Top-Down Approach of SoC.

Physical prototyping should provide early feedback in terms of design closure and helps validate the correctness of design decisions. Also physical prototyping should accurately be predicting the characteristics of the final physical implementation.

These are the some design tradeoffs which can be used to overcome SOC complexity issues to reduce them as much as possible.

- Better Design Policy
- Proper Functioning Modules
- Better Test Approach
- Designing Methods
- Stability / Flexibility
- Use of best language

3. Survey to SoC Based Systems

3.1 Earlier SoC Scope

Years ago System-on-Chip were developed to determine the increasing problems and complexity in the existing operations. Because of this many new components have been designed on the chip to support the on chip communication. But this feature also introduced many drawbacks like ironic power consumption, performance effects, cost and design time of modem cycle, on SoCs. The increasing complexity level in the applications greatly strained the communication process, which imposed bad effects on SoC design. Many efforts including academic and industrial are made to correct the SOC designs.

3.2 SoC Circuit Designs

The integrated circuit of SOC includes several channels on it. A logic device is connected with the processor local bus, peripheral devices are connected to the peripheral device bus, a memory unit, and an input/output unit and a processor local bus are connected to the bridge channels. There are many low on cost chips technologies that enable low cost structures, performance and modularity of multiprocessors SoCs.

Soperton is an on chip technology that provides standardized network interfaces, modularity, and high performance, communication link with small buffers on network-on-chip. In SoC technology Moore Law plays an important and efficient task in providing challenges in the CMOS integration capability. Basically the SoCs structure complexity is determined by viewing its bus architecture. There are many on chip technical systems like.

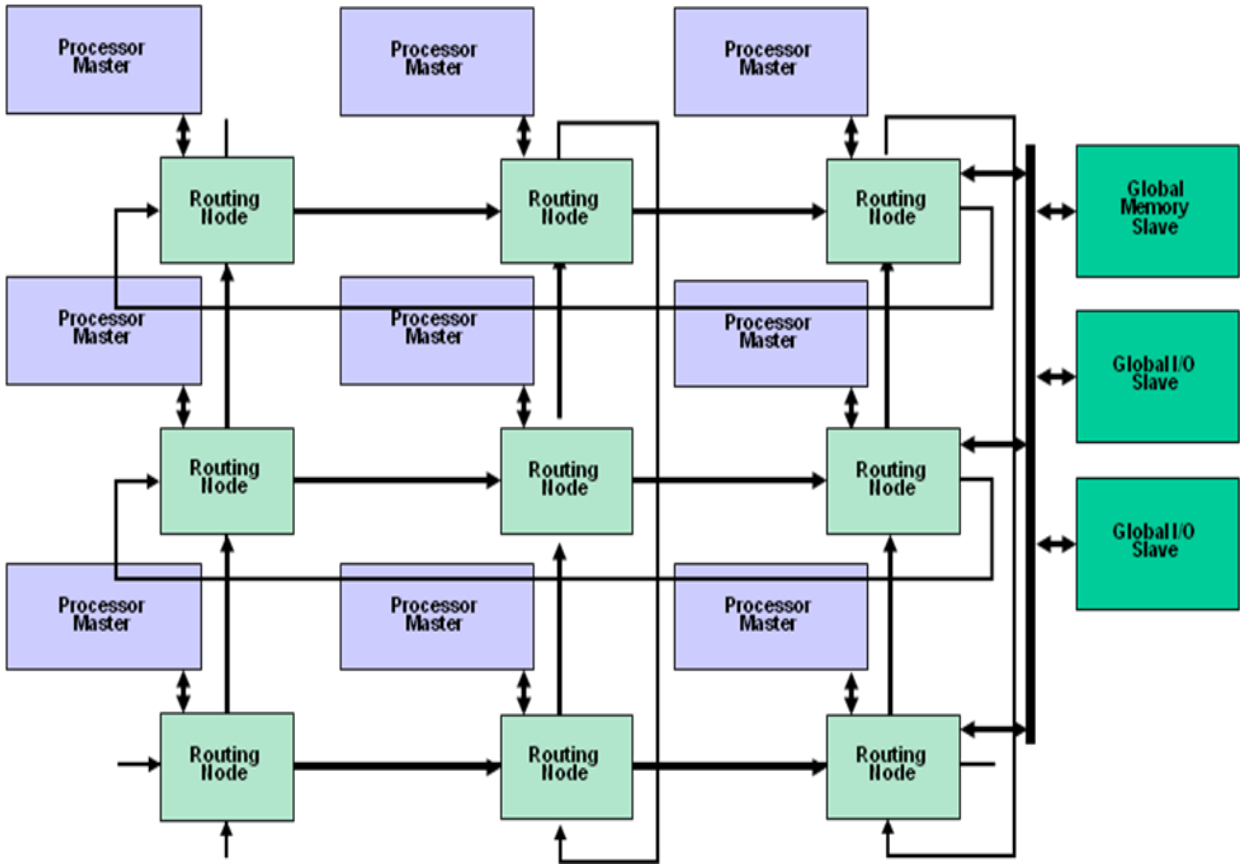

Fig. 4 Typical NoC System [1]

3.3 NoC Paradigm

It is an optical on chip communication technique. It is dealing with the trend of furnishing SoC performance, system scalability and power factors. It is doing this by replacing bus architecture to packet-based which includes network layered protocol's general view of NoC bus architecture ideology [1], [3].

These layers provide communication framework for designers. In this design IP communicates with other system SoCs through its own NoC link. These NoCs have been in use for academic and industrial research purposes for years [5]. But many existing research engines have putted claims on NOC architectures designs. But still NoC communication is commonly in use because of the less network buffering capability and packet's independence from distances [6]. These packets are subcategorized into flow a control unit which operates on flits. NoC basically follows a generic layering approach for communication. SoC is the capability to position multiple components on the single chip. They perform the best functioning for the system and play their role. Mixed system signal on chip consists of many analogous and electrical signaling features Electrical wires and circuit layering that transfer information.

a) SPIN [4]
b) CLICHE
c) Torus
d) Folded torus
e) Octagon
f) BFT

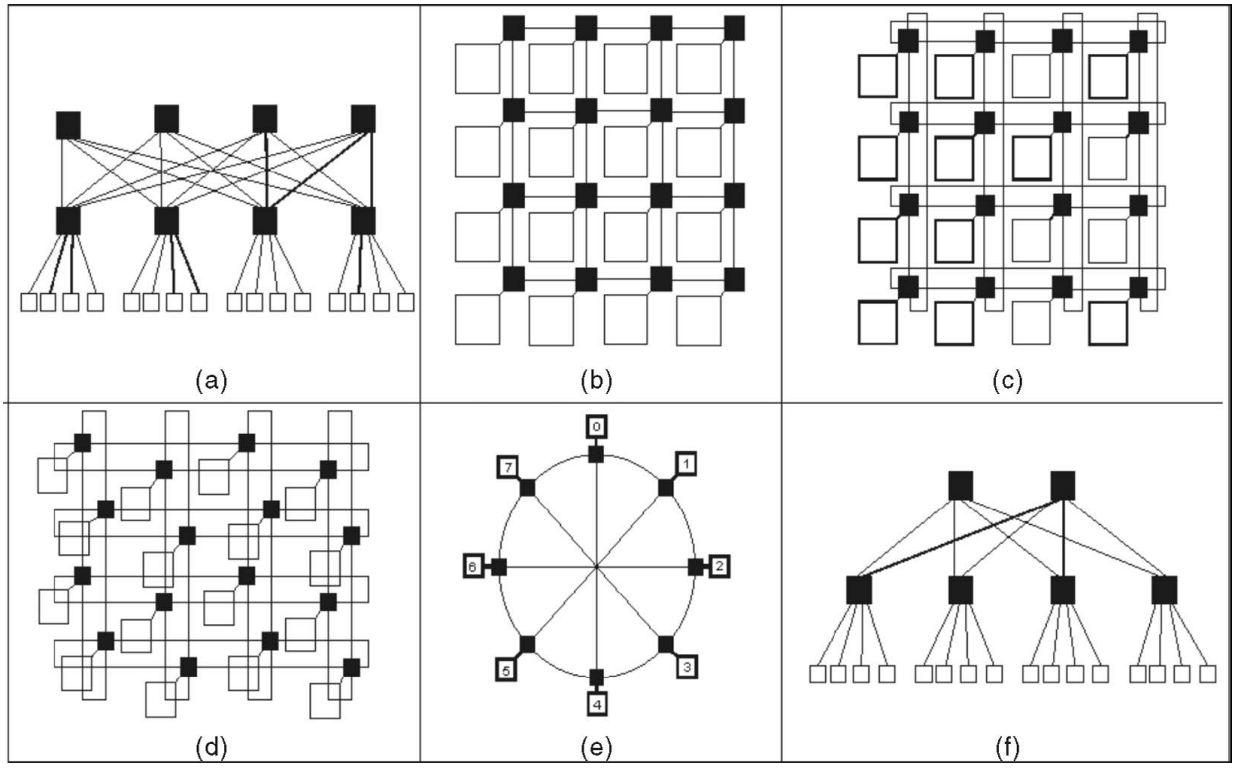

Fig. 5 Network Topologies [1]

Application layer

Which receives hardware and system calls

Presentation layer

The presentation layer basically provides a kind of surety about that the internal data communications which are being passing through are in user defined appropriate data format.

Session layer

This layer has an alternative name i.e port layer. This layer acts as a manager and is responsible for dealing/managing the setting-up and taking-down of the related association between two primarily communicating channels or end points. This processed activity is commonly known an established network connection. A logical data connection between two end points is maintained when these two points are communicating back and forth in an exchange or session consisting of some duration.

Transport Layer

This logical network layer is a collection of standard methods and standard protocols inside a communicational layered design/structural of network based components and within this structural architecture/design the transport layer is fully the in-charge for the locally data encapsulation of any running program/applications data-blocks into fixed length data-units known as data-grams or TCP data-segments which are then technically quite suitable for being able to transfer to the internal network layer infrastructure for further transmission to the required destination host machine .

Network layer

This relates with the routing scheme and topology of the system.

Data link layer

This proclaims reliable data transfer.

The network architecture specifies topology and physical interconnection of network. a network architecture operates according to a set of protocols which principally determine switching and routing and control flows. The elements of an on chip network architecture are processing components that we call are switches, nodes and physical links.

Nods: Are computational elements

Routers: Incorporate switches

Repeaters: Links that are wires and are tasked to amplify signal and to maneuver its edges

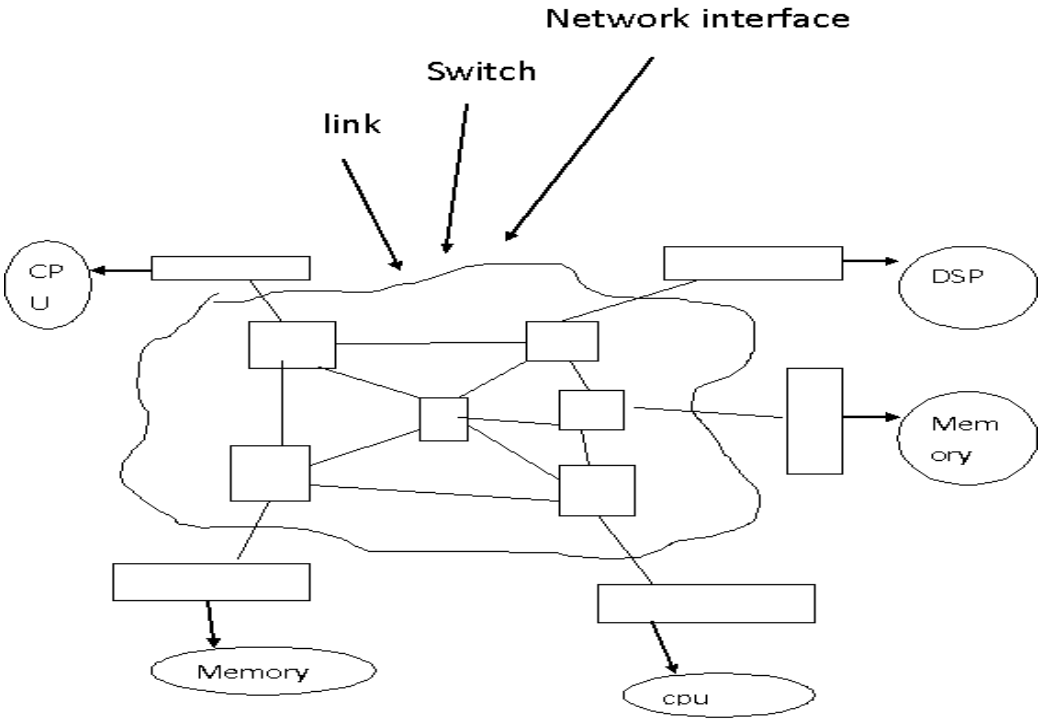

Fig. 6 Physical Interconnection of a Typical NoC.

3.4 NoC Architectures

On chip network architectures are classified into four groups

Shred Medium Networks

The transmission link is shared amongst by all nodes and single node is authorized one at time to send information

Direct Networks

Each node consists of a router and point to point links to other nodes.

Indirect Networks

Each node has a connection to a switch which has a point to point link to other switches. It is an alternate to direct networks. In indirect networks a logical connection is established by means of a set of routers or switches.

Hybrid Networks

It is a mixture of all shared medium direct and indirect networks.

Shared Medium Network

Most SOCs use shared medium architectures. It is considered the simplest possible data interconnection design/structure in which a kind of single communication medium is shared among all of the related communicating electronic devices. It allows a connection to one or more slave's .each device that is connected to the network has a network interface with requester driver and receiver. This network strategy is passive.

Hybrid Network Objectives

Include increased bandwidth with respect to shared medium networks and is being reducing the total communication distance being available between any of nodes as compared to the well known direct-networks and indirect-networks.

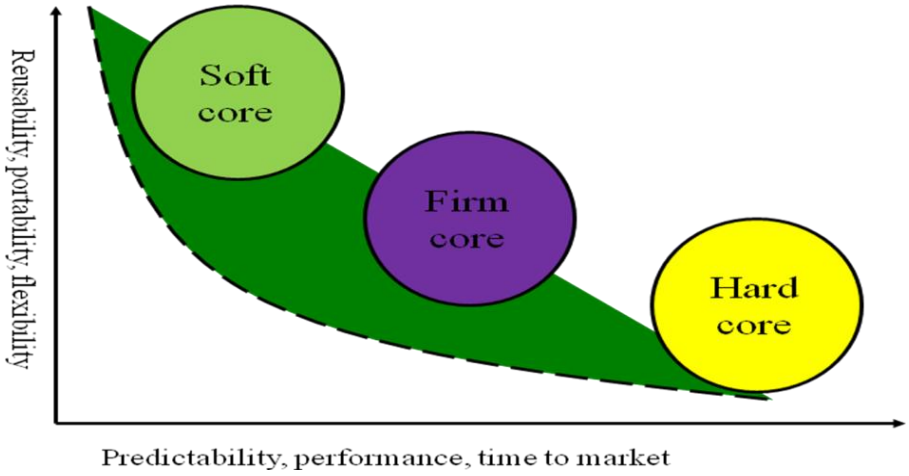

Fig. 7 System-On-Chip Cores

4. Application Areas of SoC Technology

4.1 Next Generation Medical Applications

Soc technology is serving us in many disciplines. System on chip technology provides solutions for next generation medical applications. The latest SOC technology helps designers of portable medical equipments. The market for medical electronics is growing rapidly. These electronic devices provide sophisticated solution for diagnose a disease and its treatment as well. These devices have special monitoring system that detects the required disease, for instance blood monitoring system, insulin pumps and body temperature sensors etc. Cardiac rhythm management is one example of such system. These medical applications demand high performance sensors and functionality in smallest possible time with low rated of power consumption.

Many medical equipments use single IC .These IC's are build so that they can combine analog and digital capabilities. These applications have number of fundamental design requirements .The devices which are implantable require to have long life and they should be

maintenance free. Extremely high incorporated, mixed-signal SoC solutions are absolutely ideal for medicinal OEMs, who keep a look to increase the functionality of implantable and transportable medicinal applications. These SoC provide solution to diminish size and trim down power consumption. The dexterous availability of the latest mixed-signal processes, which include smart sensor interfaces, will play a significant role in lessening the progress time of such solutions.

4.2 Chip-On-Chip Technology

Chip on chip is next emerging microarray platform. It is also known as LOCATION ANALYSIS (LA). It provides mechanism for methylation, DNA replication, DNA modification and repairing of DNA as well.

4.3 Programmable System-On-Chip

Programmable system on chip consists of configurable analog and digital blocks, a CPU subsystem, routing and interconnect. PSoC allows plug in predefined and tested IP from the PSoC library of functions, or code your own. This approach provides flexibility to introduce innovative and competitive advantages to the product.

4.4 Programmable Routing & Interconnect

It frees one to again and again routing signals to user selected pins, shedding the constraints of a fixed-peripheral controller. Global buses eliminate the need for a complicated digital-logic gate design, thus permitting signal multiplexing and logic operations [7].

4.5 Configurable Analog and Digital Blocks

The union of both analogue and digital circuitry made programmable SOC possible. Changes could be made on these blocks by configuring them. By combining several digital blocks, 16-, 24-, or even 32-bit wide logic resources can be made. The analog blocks are composed of an assortment of switch capacitor, op-amp, comparator, ADC, DAC, and digital filter blocks, which allow the complex analog signal to flow. Modification and personalization to each function could be made.

4.6 CPU Subsystem

PSoC offers a sophisticated CPU subsystem with SRAM, EE PROM, and flash memory, multiple core options and a variety of essential system resources including:

- Internal main and low-speed oscillator.
- Connectivity to external crystal oscillator for precision, programmable clocking.[Sleep and watchdog timers.
- Multiple clock sources that include a PLL.

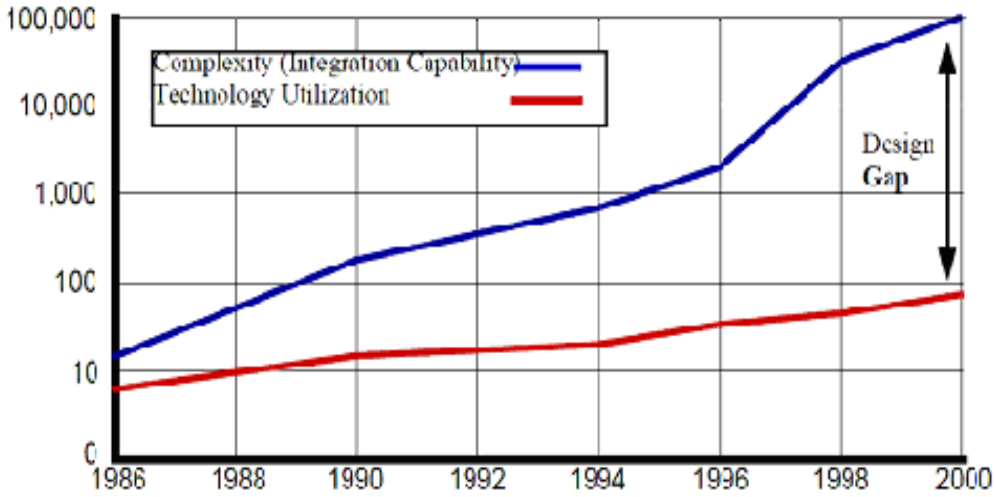

Fig. 8 Complexity vs Technology Graph

4.7 Mixed Signal System-On-Chip (SoC)

Analog and digital circuitries when placed together make the mixed signal system. This design has remarkably increased the easy going features in systems like installation, ease of use and portability. Mixed signal applications have taken a prominent ground on almost every application. The major applications have been in the fields of Sensors, Healthcare and the RF SoC. Many conventional systems have been replaced by solid state electronic systems. Almost every application and utility has taken over by the semiconductors. Examples include medical, home networking space and infotainment equipments. Engineers are now using ICs in which both analog and digital circuit is placed on single board. Mixed signal System on chip has become an inevitable solution for numerous applications. The communications to a user display handled by the processor. This makes use of low power consumption. These requirements are accomplished by the Mixed Signal devices. Wireless applications are yet another field of interest for the designers of Mixed Signal SoCs.

5. Potential Research Areas

This report gives a compact and precise overview of SoC technology. It gives idea of the relative and present consequences of SoC technology being in use today. This research has gone over its trend to search the right research terminologies. This report is the final description of the working experience of the group efforts on the topic of "System-on-Chip "technology.

5.1 SoC Objectives

The objective of soc technology is to provide a user interactive platform which could overcome much of the hazards which the early technologies had faced. This is a vast field which is still in progress with the expertise working in it. In the 20th century the opportunities were introduced to cope up the environmental needs. Later it leads to the information technology but

now soc is of the highest rank which still has not completely launched its services.soc was first introduced at higher laboratory levels and organization but now it is leading to indulge in to common personal services.soc basically is all in one technology. It is the one which embeds all of the essential operating system components on a single chip. Due to its features it is becoming more users demandable.

People want soc to provide more embedded systems on a single chip with the ease, more trust and more reachable with the society needs.soc research communities has developed many ideas so to support computer science and engineering in much better way up to the users expectations the soc is boosting the level of required investments to overcome the potential and challenges which it still is facing. The growth of soc market is obvious but the need for more is also obvious.soc has maintained reliability and compatibility of the existing systems. Circuit complexity which was the critical issue in the isolated traditional system applications is under view of designer to reduce the power loses since from manufacturing of the chip. An example of it is the wireless embedded communication system which is running with less power consumption. First soc technology was wireless internet phone that provided base for further soc based systems like common radios, decoded mixed-signals and digital signal processors (DSP) on the same chip [8].

5.2 SoC Challenges

It requires a virtual environment so to perform system verification before running the actual program. These problems may cause due to the power factor. Designers and manufacturers are now working to reduce power hazards as much as possible to make the chip more reliable. As with the soc technology the system-in-package technology is also of great fame due to its feature of vendor interoperability.

5.3 SoC Equivalent Sip Technology

Sip operates with less power consumption so it is ideal for power management scheme. As applications today demand for a big power processing in the existing system, hence it is a big challenge for the developers to fill up the user needs. Free scale architectures provide greater processing capabilities without much power consumption.

5.4 Power Management

Power management issue was aroused due to quality of regulation and conversion efficiency. This problem was aroused with the low level voltage but now it has become so one of the critical issues in multi-mode DC. In devices much of the power is consumed in digital processing. So digital circuits are improving semiconductor processes to reduce power consumption. It is facing the problems and complexity of designing, verifying and manufacturing of such chips. If the power factor will not be dealt since from the beginning, the system will not guarantee power performance.

5.5 DVFs Technology

The use of DVFS techniques can reduce the power consumption issue in SOC ships. APC can also be used with dynamic frequency. Because SOC management unit supports APC interfaces with SoC, there are two major SoC scale voltage domain HARDWARE ACCELERATOR and CPU [8], [9]. According to DVFS technology the digital processes run in the domain. If the voltage domain is large enough then multiple HMPs can be used with the clock domain. The major functions of APC are Interrupt management service. Voltage scaling manages display of frequency voltage table. The APC implements DVFS technology functions in two modes one as DVS which fetches the voltage value from DVS table. Second is power wise mode in which frequency changes and providing the new frequency to the DVFS domain.

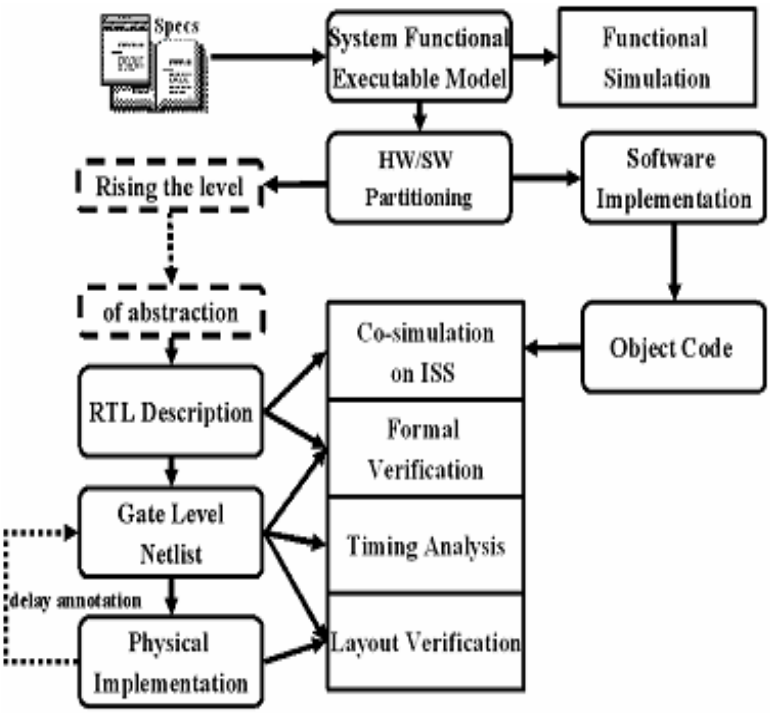

Fig. 9 Conventional SoC Design

6. SoC Design Methodology

Digital still cameras are rapidly developing with shorter time period. The major purpose is to provide better image quality, image resolution and image color scheme and from the hardware aspects to reduce power consumption, cost and greater storage capacity. Although many companies have launched many efficient technology based products but the digital camera is still behind in race with video camera. This example explains the complex designing of the digital consumer cameras. It uses best sensors, LCD, high quality lenses complex DSP systems to provide better product.

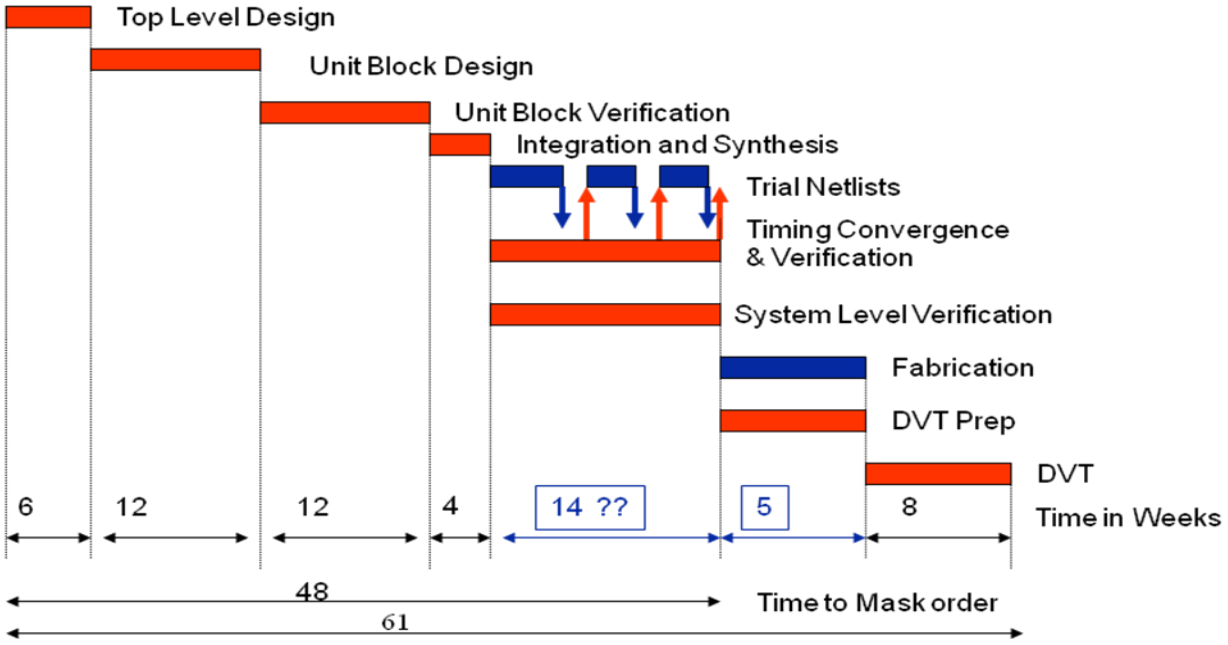

Fig. 10 Typical ASIC Based SoC Design Flow

The new polymorphic technology which was introduced by Cadence has extended the product capability to overcome the challenges of the designing [10]. It uses an image processing algorithm which first makes the recapturing options fixed and then commands for taking a new image. This polymorphic technology has used the algorithm written in C++ language which is easily understandable by most of the users.

7. Conclusion

We have presented the concept of the SOC technology which is ht vast and emerging trend for the new generations. Here we have referenced many case studies and many examples of the existing SOC based systems. As user interactions with the machines are becoming higher and higher in number so the demand for the better system support is also increasing. Soc seems to be the more advanced and more complex technology. In present we are watching integrated chip methodologies basically for computer but in future we will also see advanced videos and wireless integrated together. SoC technology is emerging domain which is being highly investigated to support high speed computing approaches. There are many issues relating with this domain which need a high level of research look. After addressing these issues the SoC technology can be fairly enhanced for future computing systems.

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