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Development of a Low-Cost, Portable, 12-Lead ECG Machine for Health-Care Centres Across Rural India

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Abstract

India being a developing country, it concentrates its resources towards indigenizing various technologies making them economically feasible to the general population. Considering that roughly half of the country dwells in villages and small towns, even basic sanitation and primary health-care facilities are virtually non-existent in far-flung reaches of the Indian sub-continent. Coupling the problems of wide-spread poverty with increase in life-style related diseases warrants a greater budgetary allocation needed for providing primary health-care across the country. Among the various life threatening diseases cardio-vascular diseases form a sizable chunk. An attempt has been made towards indigenous development of a 12-channel ECG machine beginning from first principles. This paper presents a detailed technological overview on the development of an ECG machine with special emphasis on the design aspects of the analog front-end chip. Detailed computational simulations were employed in arriving at a viable electrical design of the front-end chip which could be fabricated cost-effectively. The front-end IC has been integrated with analog and digital modules to realize a one of a kind 12-channel ECG machine within the country.

Keywords: Application specific integrated circuit; Common mode rejection ratio; Power supply rejection ratio; Ceramic leadless chip carrier

Introduction

Historical perspective

Indians are genetically at higher risk of developing heart diseases owing to the smaller dimensions of their blood vessels. Being a developing country, India lacks even basic health-care infrastructure in its far flung rural villages. With the gradual progress in development meaning life-style related diseases like heart-disease, diabetes, renal diseases etc. have taken a toll on the population. On an average 30% of Indians suffer from various cardio-vascular diseases. Latest statistics reveal that roughly 27 % of India's population falls under the below poverty line category. With the slow pace of economic growth seen in recent years India has not been able to fund rural health-care and poverty alleviation schemes with generous budgets.

Objectives

Our research is directed towards bridging the cost divide in providing much needed basic health-care for our less-fortunate countrymen living in rural India. As a precursor to providing diagnostic indicators for heart diseases, an ECG machine forms an integral piece of equipment to be installed in village health-care centres across India.

Comparative statement

Commercially available ECG machines cost roughly Rs.50, 000 per piece which is too high a price to pay for one module considering an average Indian village has roughly more that 10,000 individuals. An indigenous initiative to develop ECG machines will go a long way in providing sustained supply of basic diagnostic health-care equipment for the country.

Concept and realization

A low cost, low power and portable ECG system has been conceptualized for application in rural health care centers across the country. Being a totally indigenous initiative meant that design and development of individual components be carried out in-house. As a part of this effort, a custom designed analog front-end ASIC (Application Specific Integrated Circuit) has been conceptualized and realized in standard 0.35 micron CMOS technology. The selection of CMOS technology was from cost sensitive considerations. Commercial Bio-potential front-end Chips are incapable of acquiring more than input 8 channels simultaneously, thereby seriously inhibiting the diagnostic process resulting in false positives. One of the striking features of our system is its ability to acquire ECG signals from all 12 input leads/channels simultaneously in real time. Some of the salient features of the designed ASIC were viz. wide band-width (50 mHz-50 Hz), low RMS noise (2 μV/channel), high differential electrode offset tolerance (~50 mV) and low power dissipation (29 mW).

Summary

This paper presents an overview on the design philosophy of the ECG system encompassing the realms of IC design, embedded systems and software development. The designed front-end IC has been integrated with a digital data acquisition module comprising of 16-bit micro-controller; ADC and LCD display to realize the first proto-type of the 12-channel ECG machine.

Medical certifications

Extensive clinical trials of the 12-channel ECG machine will be carried out for qualification of the general standard *IEC 60601-1 - Medical equipment medical electrical equipment - Part 1* certification.

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Development of Front-end ASIC

Overview of electrical design

The ECG front-end IC was designed to present a wide band-width coupled with extremely low cut-off frequency making it possible to measure the S-T segment of the ECG wave which was critical in diagnosing diseases like coronary ischemia. In-built noise suppression was achieved by optimization of number of filter stages, to give an RMS input-referred noise as low as 2 μV/channel. Problems of differential electrode offset were mitigated by implementation of a *dc* cancellation stage to an extent of achieving a differential offset tolerance as high as 50 mV. Analog signal processing was implemented for generation of augmented vector signals making this system highly versatile. The total power dissipation was merely 29 mW making it possible to power the entire system through a single Lithium-Ion battery and hence rendering it portable character.

The basic electrical block diagram of the front-end ASIC is illustrated in the figure 1. It consists of three Limb lead channels (SC1-3) (SC stands for Single-Channel), six Pre-cordial (Chest) channels (C1-6), one combinational channel block (augmented vectors: aVL, aVR and aVF), input-buffers, and five current bias blocks. The limb lead inputs (LA, RA and LL) are connected via input buffers to the three single-channels (SC1-3) in a fashion illustrated in figure 1, to realize limb lead (L1, L2 and L3) and augmented vector outputs. A typical limb lead channel consists of an instrumentation amplifier (IA) coupled to a gain stage, a fourth order filter stage, gain stage (Gain=25) and finally a buffer stage. The first level instrumentation amplifier stage was designed adopting the Current-feedback (CF) topology which eliminates not only the need for matched resistors for achieving high Common Mode Rejection Ratio (CMRR) but also the need for low output impedance amplifier stages. The fourth-order filter stage, gain and buffer stages resulted proved crucial in noise reduction and boosting the signal for driving back-end circuitry (Figure 1).

Chip-level layout design

The chip-level implementation of the electrical design was performed using specialized layout design tools. Design rules specific to the 0.35 micron technology available at the particular silicon foundry had to be strictly adhered to. Foundry specific layout libraries for individual elements (resistors, capacitors and transistors) were generated for incorporation in the layout. Common centroid technique was implemented in designing the layout for the differential pair transistors in the IA. In designing a multi-channel layout electrical cross-talk related issues assume criticality. To offset these issues, the layouts were designed with inter-channel isolation with uniformity of signal flow being maintained. The total silicon area of the IC was 15.75 mm^2 (4.5 mm ×3.5 mm) packaged in standard 68 pin CLCC (Ceramic Leadless Chip Carrier) package. An illustration of the complete ASIC layout showing all layers is viewed in figure 2.

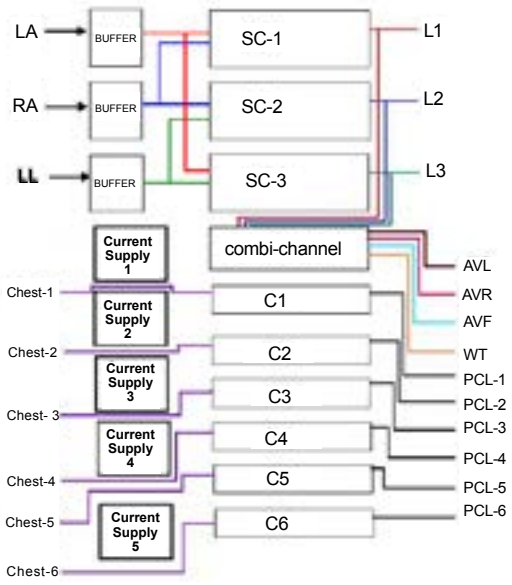

Figure 1: Electrical block diagram of the complete chip.

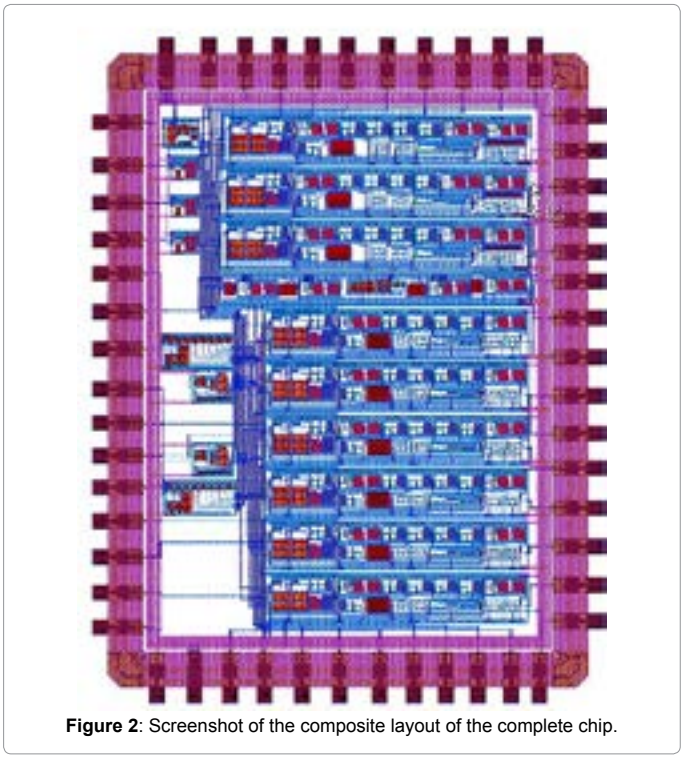

Figure 2: Screenshot of the composite layout of the complete chip.

Circuit simulations: Results and discussions

The objectives behind conducting circuit simulations were to achieve a pre-fabrication estimate of values of various circuit parameters which helped in optimization of best fit parameters. Schematic level (design stage) simulations were instrumental in optimization of the design of the individual blocks (IA, Gain, etc.). Foundry specific models libraries for individual circuit elements (MOSFETs, resistors, capacitors etc.) were employed for performing the simulations. Simulations were performed to optimize the power dissipation parameter crucial in ensuring longevity of battery life. The total power dissipation derived from simulation for the entire chip was merely 2 mW / channel, which was low enough to ensure smooth device operation for an extended period. Noise figure being another critical parameter when considering circuits designed for low power applications. The analytically derived noise voltage value was 1.85 μV/channel. Additionally, *ac* analysis simulations was carried out to derive values of gain at mid-band frequencies as well as the cut-off frequencies for both limb and Pre-cordial leads (PCL). Mid-band gain values for Limb and PCL leads were 488.32 and 243.99 respectively. The frequency band-width worked out to be 150 Hz (50 mHz-150 Hz). CMRR of the complete ASIC was 129

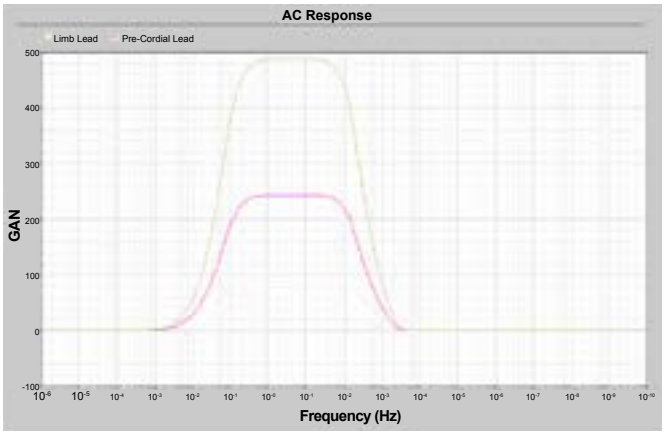

Figure 3: ac response of the Limb and Pre-cordial channels.

S. No.	Parameter	Characterization value	Analytical value	Deviation %
1	Gain for Limb Lead channel	54 dB	53 dB	1.85
2	Gain for Pre-cordial channel	48 dB	47.47	1.1
3	Power Dissipation	29 mW	18.74 mW	35
4	Band-width	50 mHz –150 Hz	50 mHz –150 Hz	0
5	CMRR	115 dB	129 dB	10.85
6	PSRR	77 dB	88 dB(+)	12.5
7	Input referred Noise / channel	2 μV	1.85 μV	7.5

Table 1: Comparison of results from characterization and circuit simulations.

dB whereas Power Supply Rejection Ratio (PSRR) was 88 dB and 52 dB respectively for positive and negative supplies respectively (Figure 3).

Electrical characterization: Results and discussions

Electrical characterization was conducted for accurate estimation of values for various dc performance parameters viz. gain, power dissipation, noise, etc. being a custom designed chip its characterization warranted the design and fabrication of a special purpose PCB. Ac parametric test of the chip performed using a square wave input. Cut-off frequency was estimated by measuring the skew and tilt in the output waveform of the chip for a square wave input. A 10% tilt in the output square waveform results in a lower cut-off frequency of 50 mHz. The average noise figure derived from characterization was 2 μV/channel (Table 1). Transient response of the chip to an input signal was extracted by giving input stimulus from an ECG signal simulator (Fluke **PS420**) and the corresponding waveforms were observed over an Oscilloscope (Figure 4).

A comparative statement on the values of the various dc and dynamic performance parameters derived from simulation versus those derived from characterization as well as the deviation between these two sets of values is tabulated in table 1. Deviation in values derived from characterization with those extracted from simulations was within 10%, except for the parameters of power dissipation, CMRR and PSRR. The power dissipation factor was higher for the practical case owing to the incorporation of passive components on the analog circuit board. The CMRR was lower owing to presence of noise from various sources like electromagnetic pick-up, power-supply noise etc. PSRR had to be low due to presence of ac ripple in the mains supply. This was minimized by supplying power from a battery pack. Moreover, electromagnetic pick-up induced common mode noise signal (50 Hz) could only be removed by applying complex averaging algorithms in the software layer of the system.

System Integration

After having achieved the desired analog specs for the fabricated ECG ASIC, the next level of development was to graduate to the overall integration of the complete ECG machine. To begin with, the patient is connected by dry electrodes to the input of the analog signal processing module consisting of the chip and related essential passive components. The extracted amplified analog signal then forms the input to the digitization module consisting of a MSP-430 microcontroller with an on-board TFT display (320 × 240 pixels). The digital module also has a built-in SD card interface feature making it a class above existing ECG machine in the market today [1-7].

The micro-controller firmware was developed in timer synchronized ADC conversion routine. Data is collected from all 12 leads simultaneously at any given time whereas the display is programmed to plot waveforms from only three input leads at any given time on account of its small form factor from constraints of portability. There is an on-board facility to switch to outputs from the next three input

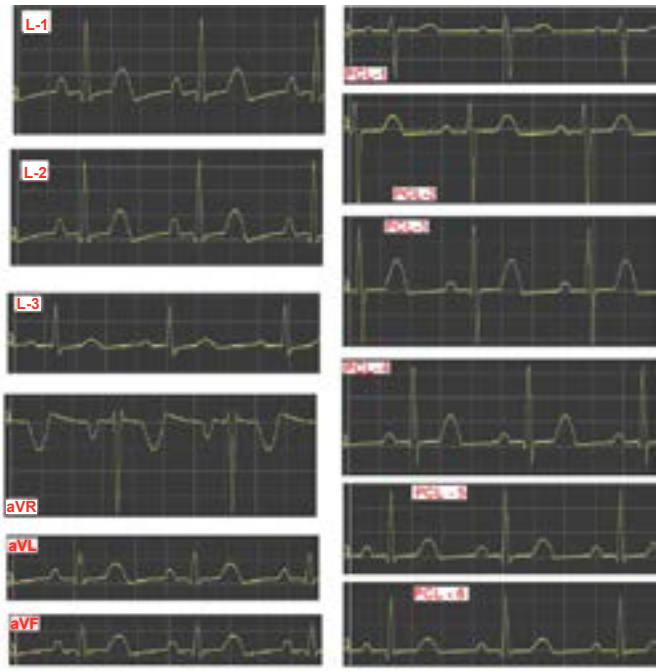

Figure 4: Photograph of the waveforms on the oscilloscope for all 12 lead channels.

Figure 5: A pictorial illustration of the ECG machine (L) and displayed waveforms from three leads(R).

leads. A photograph of the developed ECG machine with the displayed output waveforms is illustrated in figure 5. There is an on-board battery charging circuit for charging the Li-ion battery to ensure undeterred power supply.

Conclusions

Development of the first proto-type of a low cost, low power and portable ECG machine has been accomplished with a great degree of success. Analog design topologies together with chip layout design in 0.35 microns CMOS technology have been implemented. The integration of the ASIC into a complete ECG system has been carried out. From a future perspective, the system will be interfaced with an on-board thermal printer for concurrent printed output of the waveforms. A dedicated wireless interface is planned using Bluetooth communication protocol. Dedicated software for spectral analysis of the ECG signals when developed will be helpful in efficient diagnosis of various cardio-vascular diseases.

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