Design and Simulation of Nano Scale High-K Based MOSFETs with Poly Silicon and Metal Gate Electrodes

Shashank N
Sensors & Nanotechnology Group, Central Electronics Engineering Research Institute Council of Scientific and Industrial Research (CSIR), Pilani – 333031, India
shashank@ceeri.ernet.in

S Basak
Birla Institute of Technology and Science, Pilani – 333031, India
ranbasak@yahoo.co.in

R K Nahar
Sensors & Nanotechnology Group, Central Electronics Engineering Research Institute Council of Scientific and Industrial Research (CSIR), Pilani – 333031, India
nahar@ceeri.ernet.in

Abstract

High-k / Metal gate technology is emerging as a strong alternative for replacing the conventional oxynitride dielectrics and polysilicon gates in scaled MOSFETs for both high performance and low power applications. The key issues which complicates the use of high-k materials such as reduction in drain current, transconductance and mobility are resolved by replacing polysilicon by thermally stable, low work function metal gate. The advantages of using high-k over conventional SiO_2 dielectrics and metal gate over poly gate are compared. The simulation results show the reduction of gate leakage current by six orders of magnitude for HfO_2 – TiN structures compared to SiO_2 – polysilicon structures. Similarly the sub-threshold swing (1/S) is also found to decrease from 90.5mV/decade (for conventional SiO_2 structure) to 74.6mV/decade for high-k metal gate structure.

Keywords: *High-k, HfO_2, Metal gates, Poly depletion, MOSFET, Scaling.*

1. Introduction

Since the advent of MOS devices over 40 years ago, SiO_2 has been used as an efficient gate dielectric. The need for increased speed at constant power density has led to shrinking of MOSFET dimensions and as per scaling rules, the oxide thickness is also reduced in step. With scaling reaching sub-100nm technology nodes, the introduction of novel materials became inevitable as scaling of SiO_2 below 3 nm raises a serious concern in terms of tunneling current and oxide breakdown. Although optimization using nitride/oxynitride gate stacks were under pursue to lower the leakage current, still a need for better high-k materials persisted in order to solve the issues such as negative bias temperature instability and mobility lowering [1,2]. With implementation of high-k, essentially the gate leakage current was reduced by several orders, but

other issues such as thermal stability, interface layer control, increased interface charges and poly depletion still persists posing various degrees of challenges that require more R&D to overcome. Even though TiO_2 had a very high dielectric constant, due to better thermo dynamical stability with silicon, HfO_2 and ZrO_2 became most favorable among many research groups [3]. Since HfO_2 is found to form a stable interface than ZrO_2, researchers have locked on to HfO_2 as gate dielectric for present and future CMOS applications. Gate electrode is also one of the main issues related to its application in high k devices. Polysilicon which was widely used for gate electrode cannot be used for devices below 70 nm. This is due to the fact that doped polysilicon shows charge depletion effects at higher voltages which reduces the gate capacitance of devices especially made with thicker dielectric. Hence metal gate electrodes are preferred over polysilicon for devices in the nanometer regime. The other advantages of metal gate electrode over polysilicon gates are much lower gate resistance and desirable work function setting [4]. Thermally stable metal electrodes are required for compatibility with conventional CMOS high-temperature processing. Most of the low-work-function elemental metal gates (4.1 to 4.3 eV) are reactive and do not withstand conventional CMOS annealing temperatures [5]. TiN being a mid-gap material with high work function is reported to remain structurally stable to high temperatures (800–1000°C) and seems to be a promising gate metal for future technologies [6,2].

In this paper, we describe the role of gate insulator and electrode material on the performance of 0.1 μm n-MOSFETs. Some of the parameters like drain current, transconductance and mobility which degraded after replacing SiO_2 with HfO_2 in poly gate MOSFETs are found to recover when metal gate is introduced. Thus the performance optimization with TiN metal gates on HfO_2 dielectric are explored and presented in the following section.

2. Design & Simulation

Simulations are performed with a two-dimensional (2-D) device simulator, SILVACO. The physical structure of the scaled MOSFET used in our present study are designed using ATHENA considering the standard Silicon Integrated chip processing technology and the electrical characteristics are simulated using ATLAS [7]. The specifications of the Silicon substrate considered for the design are P- type Boron doped substrate with doping concentration of 3×10^{17} atoms cm^{-3} and <100> orientation. Three design structures viz. SiO_2 dielectric with Polysilicon gate (D1), HfO_2 dielectric with Polysilicon gate (D2), HfO_2 dielectric with TiN metal gate (D3) are considered to explore the advantages of HfO_2 over SiO_2 dielectric and also the advantages of metal gate over Poly on high-k materials. The simulated structures, which are based on fully scaled 100 nm gate length MOSFET's proposed in the ITRS [8], have gate length of 100 nm, with effective oxide thicknesses (EOT) of 3 nm. The dielectric constant of HfO_2 gate dielectric was considered to be 20 [9]. Steep retrograde channel doping is used with surface doping concentration of 1.01×10^{18} cm^{-3} and a peak concentration of 1.72×10^{19} cm^{-3} at a depth of 25 nm. The impact of the channel profiles on the device performance has been discussed in [10]. The source/drain extensions and deep source/drain junction depths are 45 and 75 nm, respectively. Tungsten Silicide is used at source drain contacts to reduce the sheet resistance. After LDD (Low Doped Drain) implant the effective channel length was found to be 70nm. The

gate work-functions for n^+ doped polysilicon gate and TiN are chosen to be 4.17 and 4.5 respectively. The surface states were considered to be one order less in SiO_2 based structures (5 x 10^{10} Charges/cm^2) as compared to structures with HfO_2 as gate dielectric (5 x 10^{11} Charges/cm^2) as the basic charge trapping is much more pronounced with the metal-oxide insulators than with silicon dioxide. The threshold Voltage of all the design structures is kept at 0.5V. Quantum models are introduced during the simulation of D1structure because of very thin (~3nm) SiO_2 layer. Effective channel mobility for all the design structures are extracted at 1 nm below the dielectric-silicon interface. The reason for selecting such probing location is that good numbers for mobility (fact that some of the mobility numbers were comparable to the ones published from experimental results in the literatures) were obtained when probed below 1 nm from the interface [11],[12]. In our present work we have used the modified WATT model to simulate the mobility. Simple WATT model is a Transverse field model applied to surface nodes only. Modified WATT model is the extension of WATT model which can also be applied to non surface nodes. Modified WATT model applies constant perpendicular electric field effects and is best suited for planar MOS devices. The modified Watt model includes all the effects of phonon scattering, surface roughness scattering and charge impurity scattering effects caused by the inversion charge carriers and the ions located in the oxide and interfaces [13]. This was in line with our requirements. Hence this model was selected specifically to show the scattering effects due to interface charges at high-k/Si interface. The schematic of one of the design structures (D3) is as shown in Figure 1.

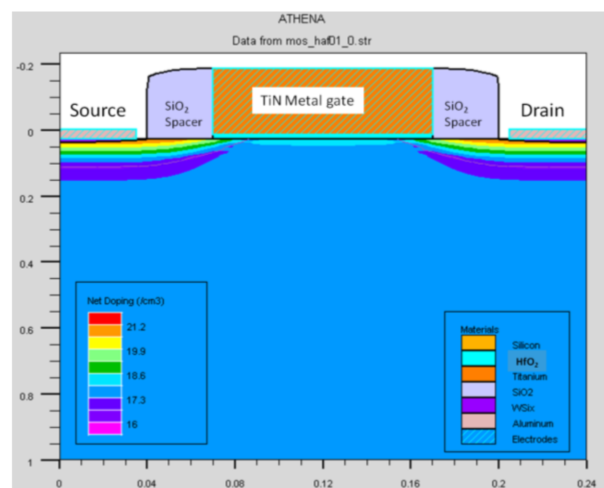

Figure 1. Design structure of 100nm channel length MOSFET with HfO_2 dielectric and TIN metal gate.

3. Results & Discussions

The role of HfO_2 and TiN in scaled MOSFETs are evaluated by comparing with the simulated results of conventional SiO_2 - polysilicon MOSFET structure. The channel was doped

with boron concentration of 9x10^{10} cm^{-2} to maintain a threshold voltage (V_T) of 0.5 V in D1 structure. When the SiO_2 dielectric layer was replaced with HfO_2, the V_T reduced to 0.04V due to the physically thicker dielectric layer and the channel doping was increased to 3.8x10^{13} cm^{-2} to maintain V_T of 0.5 V in D2 structure. This increase in boron concentration at the channel causes the decrease in the Drain saturation current (I_{Dmax}) in D2 as shown in Figure 2.

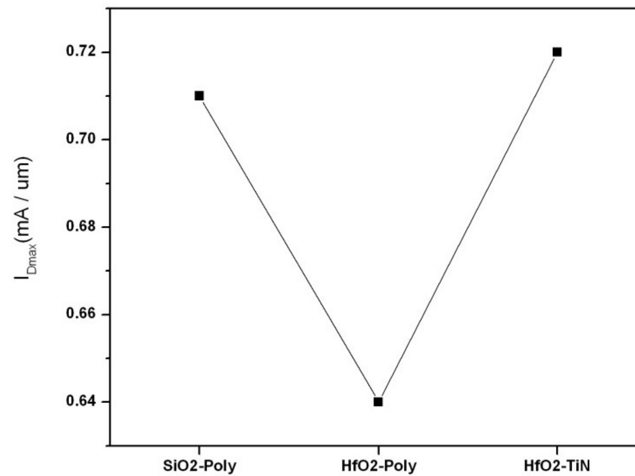

Figure 2. Drain current for D1, D2 and D3 structures

The effect of poly depletion is also said to be more pronounced with thicker high-k dielectric as poly depletion forms a low-k layer on top of a high-k layer. This leads to electric field divergence which seriously degrades the performance of short channel devices [14, 15]. The structure D3 has a metal gate instead of a poly gate. TiN being a mid gap metal and with a higher work-function than polysilicon gives a higher V_T. The channel doping of D3 structure was reduced to 1.65 x10^{13} cm^{-2} from 3.85 x10^{13} cm^{-2} as compared to D2 structure. This reduction in channel doping was necessary in order to maintain the threshold voltage at 0.5 V. The reduced channel doping with TiN metal gate along with Steep retrograde profile is found to give a higher drain current [16] as observed in Figure 2. The absence of poly depletion which reduces the effective thickness of the dielectric may also account for a higher on current in metal gate MOSFETs.

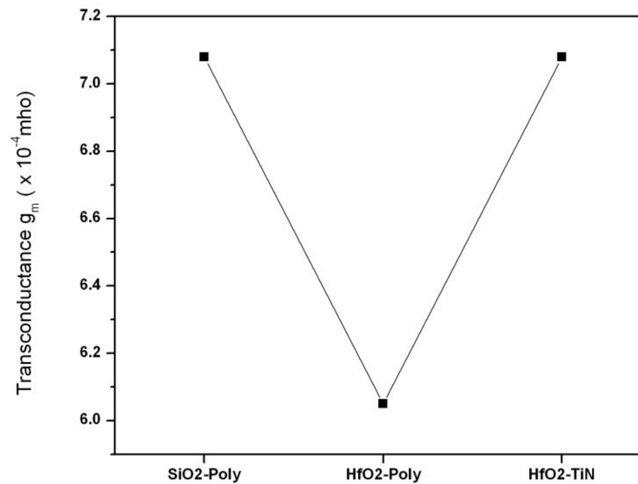

Figure 3. Transconductance for D1, D2 and D3 structures

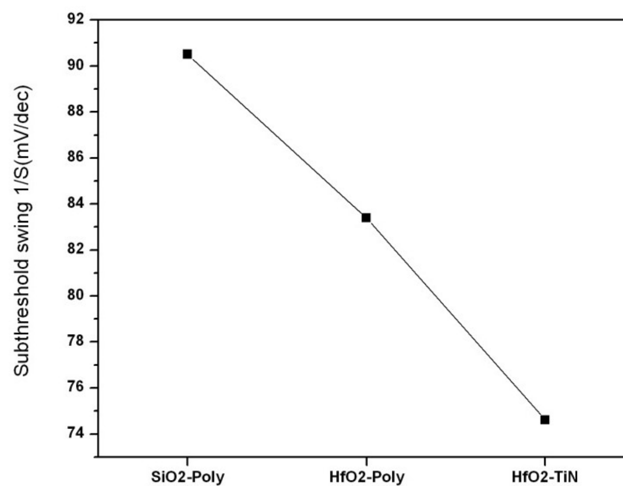

Figure 4. Sub-threshold Swing for D1, D2 and D3 structures

The transconductance is found to be 7.08 $x10^{-4}$ mho for both D1 and D3 structures and decreases to 6.05 $x10^{-4}$ mho for D2 structure. Figure 3 shows the variation in transconductance which seems to be in analogous with the variations in the drain current. Sub-threshold characteristic of a MOSFET is an important parameter which determines the holding time in dynamic circuits as well as the static power dissipation in static CMOS circuits. From Figure 4 it can be observed that the sub-threshold swing (1/S) decreases from 90.5 mV/dec to 83.3 mV/dec when SiO_2 is replaced with HfO_2 dielectrics. This may be due to reduction in leakage current between drain and gate while using high-k dielectric material [17]. The reduction in 1/S values with HfO_2 can also be attributed to heavy threshold adjust implants which blocks shallow paths for punch-through current thereby reducing 1/S in short channel devices [16]. The 1/S is found to further reduce to 74.6mV/dec with the replacement of poly with TiN metal gate. This sort of behavior has also been reported by other researchers [18].

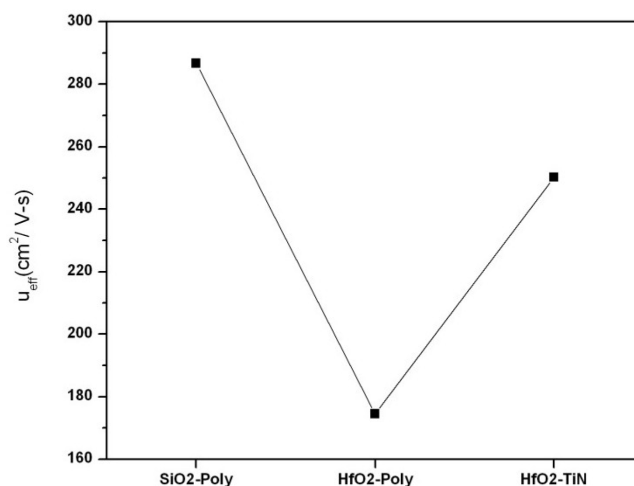

Figure 5. Effective mobility for D1, D2 and D3 structures

Among various challenges presented by high-k gate oxides, mobility degradation has received the utmost attention as it proposes a serious concern when it comes to MOSFET performance. The mobility numbers specified in the Figure 5 are the peak values observed from the mobility vs electric field curves. From Figure 5 it can be observed that there is a large fall in the mobility of D2 structure compared to D1 structure. Several factors contribute to the mobility degradation – the HfO_2/Si interface which acts as trap rich sites, higher channel doping for threshold adjustment which increases the transverse electric field [20] etc. All these factors lead to increased coulomb and phonon scattering thereby slowing down the movement of electrons and holes in the channel. Coulomb scattering due to high densities of interface charges and phonon scattering due to soft optical phonons are the major factors which limit the mobility in high-k devices [21, 22]. Metal gates on high-k are found to be a key element in future to reduce phonon scattering to improve mobility [23]. From our simulated results it can be observed that the mobility improves again with metal gate structure D3. The midgap TiN metal gate with higher free electron density is said to reduce the phonon scattering compared to polysilicon gates with lower concentrations of free electrons. The TiN gate effectively screens and reduces the surface phonons from coupling to the inversion channel, whereas depleted poly-Si gate is less effective [24].

The large decrease in gate leakage of six orders of magnitude is found when the conventional SiO_2 – polysilicon (D1) structure is replaced with HfO_2 – TiN (D3) structures and is shown in Figure 6. The reduction in gate leakage current in high-k based devices can be attributed to the physically thicker dielectric which reduces tunneling currents. Further reduction in gate leakage current in D3 structures compared to D2 structures can be attributed to the elimination of poly depletion which is also said to play a key role in improving the figure of merit for leakage reduction. It is also reported by few researchers that the formation of defects at the polysilicon – HfO_2 interface during poly deposition and activation annealing leads to increased gate leakage in polysilicon gated transistors [25].

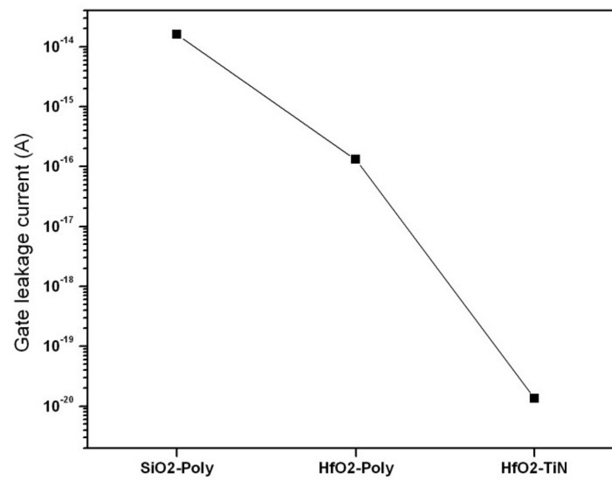

Figure 6. Gate leakage current for D1, D2 and D3 structures

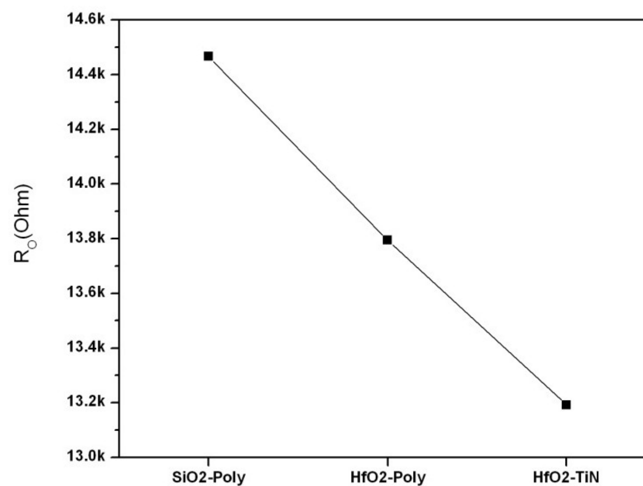

Figure 7. R_O for D1, D2 and D3 structures

The increasing use of Power MOSFETs in portable electronics and telecommunications calls for designs which ensure low ON Resistance (Ro). Ro is one of the important characteristics of a Power MOSFET which can be defined as the total resistance encountered by a drain current as it flows from the drain terminal to the source terminal. For devices to have higher current carrying capability in smaller packages, it would be advantageous to have MOSFET structures with reduced Ro [26]. From Figure 7 it can be observed that the Ro reduces from 14.4KΩ for D1 structure to 13.1KΩ for D3 structure showing the promising nature of High-k / Metal gate technology. The simulated results of D1, D2 and D3 structures with all figures of merit are summarized in Table 1.

Table 1. Simulated Results of Various MOSFET Structures with Polysilicon and Tin Metal Gates

Parameters / Models	**SiO_2 – Poly (D1)**	**HfO_2 – Poly (D2)**	**HfO_2 – TiN (D3)**
Interface charges (cm^{-2})	5×10^{10}	5×10^{11}	5×10^{11}
Threshold Voltage (V)	0.5	0.5	0.5
Drain current (mA/µm)	0.71	0.64	0.72
Transconductance ($\times 10^{-4}$ mho)	7.08	6.05	7.08
Subthreshold swing (mV/decade)	90.5	83.39	74.61
Effective mobility (cm^{-2}/V-s)	286.66	174.45	250.19
Gate leakage current (A)	1.59×10^{-14}	1.31×10^{-16}	1.34×10^{-20}
R_0 (Ohms)	14465	13794	13191

4. Conclusions

MOSFET structures with 100nm gate length were designed and simulated to study the role of dielectric and gate material on the device performance. The performance of the three structures SiO_2 dielectric with Polisilicon gate (D1), HfO_2 dielectric with Polisilicon gate (D2) and HfO_2 dielectric with TiN metal gate (D3) were compared and it was found that some of the parameters like drain current, transconductance and mobility which degraded with high-k dielectric recovered back by replacing polysilicon by metal gate. Large reduction in gate leakage and subthreshold swing projects the high k – metal gate technology to be a strong alternative for future nano scale MOS devices. With technological advances and enormous use of battery operated gadgets, the requirement for a low ON resistance also seems to be satisfied with High k - Metal gate technology.

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References

[1] Sugiyama,Y., Pidin, S., Morisaki, Y. (2003). Approaches to using Al_2O_3 and HfO_2 as gate dielectrics for CMOSFETs. Fujitsu Sci. Tech. J. 39, 94-105.

[2] Guha, S., Narayanan, V. (2009). High-κ/Metal Gate Science and Technology. Annu. Rev. Mater. Res., 39, 181–202.

[3] Hubbard, K.J., Schlom, D.G. (1996). Thermodynamic stability of binary oxides in contact with silicon. J.Mater.Res, 11, 2757-2776.

[4] Chatterjee, S., Kuo, Y., Lu, J., Tewg, J.Y., Majhi, P. (2006). Electrical reliability aspects of HfO2 high-k gate dielectrics with TaN metal gate electrodes under constant voltage stress. Microelectronics Reliability, 46, 69–76.

[5] Cabral, C.J., Lavoie, C., Ozcan, A.S., Amos, R.S., Narayanan, V. (2004). Evaluation of thermal stability for CMOS gate metal materials. J. Electrochem. Soc. 151, F283–287.

[6] Kerber, A., Cartier, E., Degraeve, R., Roussel, P.J., Pantisano, L., Kauerauf, T., Groeseneken, G., Maes, H.E., Schwalke, U. (2003). Charge Trapping and Dielectric Reliability of SiO_2–Al_2O_3 Gate Stacks with TiN Electrodes. IEEE Transactions on Electron Devices, 50, 1261-1269.

[7] ATHENA and ATLAS user's manual, SILVACO © corporation, USA

[8] ITRS Roadmap 2007, San Jose, CA: Semiconductor industry association.

[9] Sen, B., Sarkar, C., Wong, H., Chan, M., kok, C.W. (2006). Electrical characteristics of high-k dielectric film grown by direct sputtering method. Solid State Electronics, 50, 237-240.

[10] Inani, A., Rao, V.R., Cheng, B., Woo, J.C.S. (1999). Gate stack architecture analysis and channel engineering in deep sub-micron MOSFET's. Jpn. J. Appl. Phys., 38, 2266-2271

[11] Casse, M., Thevenod, L., Guillaumot, B., Tosti, L., Martin, F., Mitard, J., Weber, O., Andrieu, F., Ernst, T., Reimbold, G., Billon, T., Mouis, M., Boulanger, F. (2006), Carrier Transport in HfO_2/Metal Gate MOSFETs: Physical Insight Into Critical Parameters, IEEE Transactions on Electron Devices, vol. 53, no. 4, pp. 759-768.

[12] Lime, F., Oshima, K., Casse, M., Ghibaudo, G., Cristoloveanu, S., Guillaumot, B., Iwai, H, (2003), Carrier mobility in advanced CMOS devices with metal gate and HfO_2 gate dielectric, Solid state electronics 47, pp.1617-1621.

[13] J T Watt, Ph.D. Thesis, Stanford University, 1989.

[14] Cheng, B., Cao, M., Voorde, P.V., Greene, W., Stork, H., Yu, Z., Woo, J.C.S. (1999). Design Considerations of High- Gate Dielectrics for Sub-0.1µm MOSFETs. IEEE Transactions On Electron Devices, 46,

[15] Cheng, B., Cao, M., Rao, V.R., Inani, A., Voorde, P.V., Greene, W.M, Stork, J.M.C., Yu, Z., Zeitzoff, P.M., Woo, J.C.S. (1999). The Impact of High- Gate Dielectrics and Metal Gate Electrodes on Sub-100 nm MOSFETs. IEEE Transactions on Electron Devices, 46, 1537-1544

[16] Maitra, K., Misra, V. (2003). A Simulation Study to Evaluate the Feasibility of Midgap Workfunction Metal Gates in 25 nm Bulk CMOS. IEEE Electron Device Letters, 24, 707-709.

[17] Srivastava, A., Sarkar, P., Sarkar, C.K. Effect of High-k Gate Dielectrics on Channel Engineered Deep Sub-micrometer n-MOSFET Device, Proc. 26th International Conference On Microelectronics (MIEL 2008), 507-510.

[18] Tarr, N.G., Walkey, D.J., Rowlandson, M.B., Hewitt, S.B., Macelwee, T.W., (1995). Short-channel effects on MOSFET Subthreshold swing. Solid State Electronics, 38. 697-701.

[19] Wang, X., Shahidi, G., Oldiges, P., Khare, M. (2008). Device Scaling of High Performance MOSFET with Metal Gate High-K at 32nm Technology Node and Beyond IEEE Xplore, 309-312.

[20] Mohapatra, N.R., Desai, M.P., Narendra, S.G., Rao, V.R. (2002). The Effect of High-K Gate Dielectrics on Deep Submicrometer CMOS Device and Circuit Performance. IEEE Transactions on Electron Devices, 49, 826-831.

[21] Zhu, W., Han, J.P., Ma, T.P. (2004). Mobility Measurement and Degradation Mechanisms of MOSFETs Made With Ultrathin High-k Dielectrics. IEEE Transactions on Electron Devices, 51, 98-105

[22] Fischetti, M., Neumayer, D., Carttier, E. (2001). Effective electron mobility in Si inversion layers in MOS systems with a high-k insulator: The role of remote phonon scattering. J. Appl. Phys., 90, 4587–4608.

[23] Weber, O., Casse, M., Thevenod, L., Ducroquet, F., Ernst, T., Deleonibus, S. (2006). On the mobility in high-k metal gate MOSFETs: Evaluation of the high-k phonon scattering impact. Solid-State Electronics, 50, 626–631.

[24] Chau, R., Datta, S., Doczy, M., Doyle, B., Kavalieros, J. (2004). High-k/Metal–Gate Stack and Its MOSFET Characteristics. IEEE Electron Device Letters, 25, 408-410.

[25] Takahashi, K., Manabe, K., Morioka, A., Ikarashi, Yoshihara, T., Watanabe, H., Tatsumi, T. (2005). High-Mobility Dual Metal Gate MOS Transistors with High-k Gate Dielectrics. Japanese Journal of Applied Physics, 44, 2210–2213.
[26] Fresart, E.D., Tam, P., Tsoi, H.Y. (2000). Power MOSFET device having low ON-resistance and method" US patent 6,084,268.