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Joint viterbi detector/decoder for satellite communications

Chan Kheong Sann, Ashish James and **Sari Shafidah**
Data Storage Institute (DSI), Singapore

Satellite broadband communication today uses the DVB-S2 second generation standard proposed and developed through the DVB consortium project in 2003. The DVB-S2 standard uses a combination of a forward error correction (FEC) with multiple code rates, and multiple modulation modes giving a range of spectrum efficiencies ranging from 0.5 to 4.5 bits per transmitted symbol. The FEC scheme used is a combination of BCH and LDPC codes with combined code rates of 1/4, 1/3, 2/5, 1/2, 3/5, 2/3, 3/4, 4/5, 5/6, 8/9 and 9/10. The modulation schemes on the other hand could be one of QPSK, 8PSK, 16APSK or 32APSK for each frame. The Joint Viterbi Detector/Decoder (JVDD) is a recently proposed scheme that performs detection and decoding jointly over an encoded ISI base-band channel, and is a competitor to the LDPC decoder operating over the same channel. Alternatively, the ISI channel can be replaced by a modulation scheme that does encoding and modulation prior to the transmission, as in the case of the DVB-S2 standard. This makes the JVDD a candidate for replacing the demodulator and decoder in a DVB-S2 receiver. Previous work over an AWGN/ISI channel has seen the JVDD outperforming the LDPC decoder at shorter codeword lengths. In this work we present simulation results benchmarking the JVDD against the LDPC iterative decoding scheme at the range of code rates and modulation schemes used in the DVB-S2 standard.

Biography

Chan Kheong Sann obtained his Bachelor's degree from Northwestern University, Illinois and his PhD from National University of Singapore in Electrical Engineering. He has been working at the Data Storage Institute, a Singapore Government A*STAR research institute for 16 years and is currently the leader of the coding and signal processing team. He is currently leading is an NRF funded project from the Singapore government investigating the JVDD for satellite communications.

chan_kheong_sann@dsi.a-star.edu.sg

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