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Visual TCAD simulation of total ionizing dose effects on advanced CMOS devices for space applications

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This paper focuses on total ionizing dose (TID) effects in devices and ICs based on CMOS bulk technology. The accumulation of fixed oxide charge (Not) at silicon dioxide, interface trap charges (Nit) at substrate/silicon dioxide interface, shallow trench isolation (STI) layer for scaled CMOS devices based ICs to be operated in space radiation environment has been explored. The impact of radiation on threshold voltage (Vth), radiation induced leakage current (RILC) is shown in Fig. 1. The charge carrier density/concentrations for various dose levels up to 500 krad were presented/depicted for 65 nm NMOS transistors in space environment is shown in Fig. 2. On the basis of simulation results, various space radiation effect related parameters including accumulation/depletion of radiation induced charges at silicon dioxide; substrate/silicon dioxide interface for scaled CMOS bulk devices to be operated in space radiation environment has been reported. On the basis of simulation results, the TID robustness analysis for advanced CMOS technologies was accomplished up to 500 Krad (Si) and analysed for aluminum shield to attenuate the dose distribution to acceptable levels during mission duration as shown in Fig. 3. The correlation between the impact of technology scaling and TID robustness in space radiation environment with various dose levels were established utilizing Cogenda's Visual TCAD, Genius device simulator programs and OMERE-TRAD package.

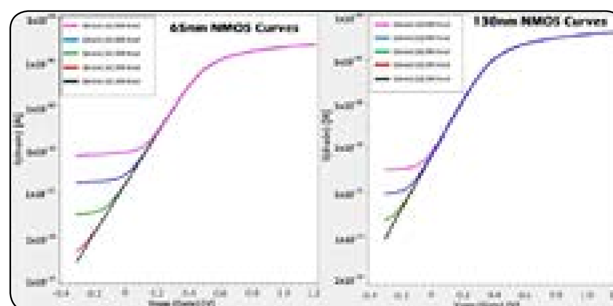

Figure 1: (a)-(b): Id-Vg Characteristics curve for NMOS irradiated to 500 krad(Si) a) 65nm b) 130nm

Biography

Muhammad Nabeel Hanif has the qualifications of Master in Physic. For the last 10 years, he has been working in Materials and Radiation Effects group in Satellite Research and Developement Center, SUPARCO. He has practical experience in analyzing/characterizing the radiation response of on-board electronics devices for satellite applications.

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