

## Multiple cell upsets rate estimation for 65 nm SRAM bit-cell in space radiation environment

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This report addresses the multiple cell upsets in SRAM based on 65 nm bulk CMOS technology node. Aggressive downscaling trends in CMOS technology has resulted in decrease of device feature size, power supply voltage and placement of MOS transistors in close proximity to substantially reduce the chip area. If 65 nm SRAM bit-cell is struck by high LET particle in close proximity outside bit-cell area, it was found that stored information can be reversed due to charge sharing between the closely place MOS transistors in deep submicron technologies. Therefore, multiple memory cells can be affected by energetic single particle strike. We report multiple cell upsets (MCUs) cross-section (figure 1) and contribution of multiplicity of MCU events in single event rate (SER) (figure 2) calculated with MUSCA SEP3 toolkit with typical aluminum spot shielding of 2.54 mm physical mechanism simulation. In order to characterize the radiation hardness of scaled CMOS devices, EDA simulation tools such as MUSCA SEP3 was utilized for MCU rate prediction whereas space radiation environment was estimated with the help of OMERE-TRAD software. The contribution of different sources of space radiation into total SER is shown in figure 3.

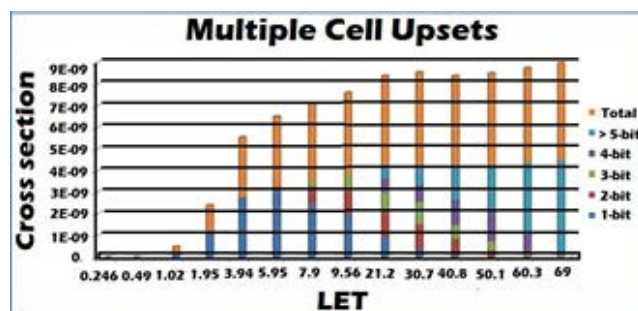


Figure 1. MCUs cross-section for 65nm SRAM device

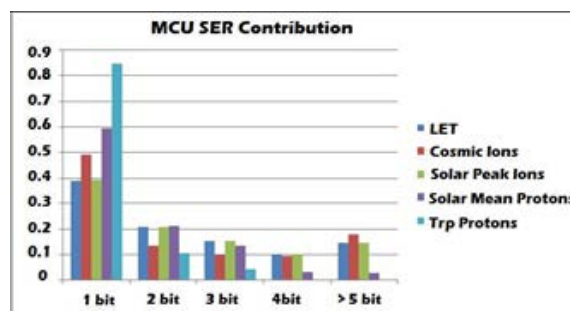


Figure 2. Multiplicity of events for MCU SER at LEO radiation environment for SRAM

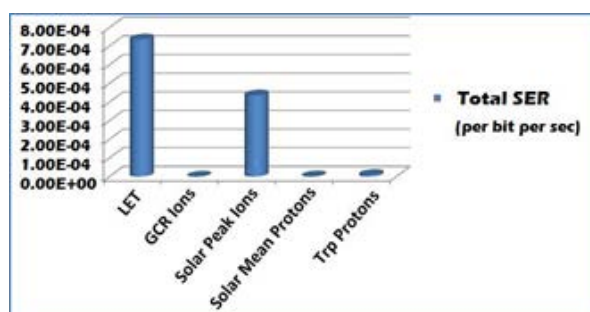


Figure 3. Contribution of protons/heavy ions to MCUs SER at LEO for SRAMs

## Biography

Nikolay G Chechenin is a Professor and Head of Division of Atom and Nuclear Physics and Laboratory of Nanostructures and Radiation effects at Skobeltsyn Institute of Nuclear Physics of Lomonosov Moscow State University. He runs several projects, including effects of space radiation on on-board electronics.

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