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Technologies for high speed III-V optical links on silicon optoelectronics

Devendra K. Sadana, Ning Li, Can Bayram, Kuen-Ting Shiu and Cheng-Wei Cheng
IBM Research, USA

Optical interconnects for high speed computing and data centres are being pursued actively. We discuss progress and challenges in several optical interconnect technologies for Si chips: 1. the VCSEL approach which utilizes discrete III-V lasers and detectors 2. integrated Si photonics which utilizes off-chip III-V lasers with co-integrated Ge detectors and 3. monolithically co-integrated Si/III-V which has epitaxially grown III-V laser and detector on Si.

1. VCSEL based optical links: Recent advances in VCSEL based optical interconnects have shown that bit rates in excess of 300 Gb/s in a ~5.2x5.8 mm^2 foot print can be achieved. Such optical interconnects will have huge impact on high performance computing and high speed data centres. However, the ultimate optical interconnect density is limited by the size of discrete optical components attached to the chip. The interconnect also requires packaging processes such as bonding and alignment which adds to the overall manufacturing cost.
2. Silicon photonics: Such optical interconnects are fully compatible with the silicon CMOS process and show remarkable performance. For example, a CMOS receiver with a Ge detector has been shown to operate error-free at 40 Gbps using 90 nm CMOS process. Integration of this interconnects technology for future high performance computing is being actively pursued. Since an off chip laser is typically required here, it impacts the design flexibility. Although lasers can be integrated on chip by wafer bonding, the overall manufacturing cost is increased.
3. Monolithic integration: The most appealing but challenging approach is to integrate optical components epitaxially on a silicon chip monolithically. This approach allows III-V lasers, photo detectors, and modulators to be integrated in silicon CMOS adjacent to each other with an extremely small footprint defined lithographically. Successful implementation of Si/III-V co-integration will increase the degree of freedom in interconnect design architecture, reduce packaging and processing cost while still maintaining a high density of interconnects, and potentially improve the performance of the optical link.

Biography

Devendra K. Sadana obtained his Ph.D. from IIT, New Delhi in 1975. He has worked at the University of Oxford, England, University of California, Berkeley, Microelectronics Center of North Carolina, and Philips Research Labs, Sunnyvale, CA during 1975-87 in various capacities. He joined IBM Research in 1987 where he is currently a senior staff & manager of the Advanced Substrate Research group. His research work covers research in Si and III-Vs including ion implantation, advanced epitaxy, SOI materials, photovoltaics, CMOS technology among many others. He has published over 200 journal/conference papers and is a co-inventor of over 300 issued/submitted patents.

dksadana@us.ibm.com