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An 8-channel neural spike feature extraction chip for large-scale neural signal recording in 0.18 μm CMOS**Peng Li, Xu Zhang, Weihua Pei and Hongda Chen**

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This paper proposes a low power and efficient neural spike feature extraction chip for large-scale neural signal recording. The communication module, control module and algorithm module are integrated in this chip. To lower power consumption, the algorithm module is designed based on an efficient online feature extraction algorithm (the Dual Vertex Threshold (DVT) and the Minimum Delimitation (MD)), and multiplexing structure is widely used in this chip design, which is beneficial to reduce the area of proposed chip. Fabricated with the 0.18 μm N-well CMOS 1P6M technology, power consumption of this chip is only 5.6357 $\mu\text{W}/\text{channel}$ in 1V voltage supply and the neural signal transmission bandwidth is reduced by 98.38%.

Biography

Peng Li has received BS degree in Electronic Science and Technology from Tianjin University in 2011 and PhD degree in Microelectronics and Solid-State Electronics at Institute of Semiconductors, Chinese Academy of Sciences in 2016. Currently, he is working at Institute of Semiconductors, Chinese Academy of Sciences as an Assistant Professor. His research is focused on signal processing and digital integrated circuit design for biomedical applications.

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